IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application No.: 10/813,857	§	Examiner:	Eland, Shawn
Filed: March 31, 2004	§	Group/Art Unit:	2188
Inventor(s):	§	Atty. Dkt. No:	5681-13501
Robert E. Cypher	§	Confirm No.	5571
	§		
	§		
	§		
Title: Multi-Node System with Response Information in Memory	§		
	§		
	§		
	§		
	§		
	§		
	§		

REPLY BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir/Madam:

In response to the Examiner's Answer of March 25, 2008, Appellant presents this Reply Brief.

I. STATUS OF CLAIMS

Claims 1-48 are pending. Claims 1-48 are rejected under 35 U.S.C. § 102(b). It is these rejections that are being appealed.

II. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1-48 are rejected under 35 U.S.C. § 102(b) as being anticipated by Liencres et al. (U.S. Patent No. 5,434,993).

III. ARGUMENT

First Ground of Rejection:

Claims 1-48 are rejected under 35 U.S.C. § 102(b) as being anticipated by Liencres. Appellant traverses this rejection for at least the following reasons.

Independent claims (by number):

Appellant respectfully submits that each of claims 1, 17, and 33 recites features not taught or disclosed by Liencres. For example, claim 1 recites features including: "each node includes a plurality of active devices, a memory subsystem, and **an address network** and **a data network respectively** configured to convey address packets and data packets **between** the plurality of **active devices** and the **memory** subsystem;" and "wherein the node is configured to store **a node identifier** for the coherency unit, wherein the node identifier **identifies a different node** of the plurality nodes **in which the coherency unit is in a modified global access state.**"

In the Examiner's Answer dated March 25, 2008, the Examiner rebuts Appellant's arguments regarding whether element 33 in Liencres could be interpreted to be Appellant's claimed address and data networks. More particularly the Examiner disagrees with Appellant as to whether the claim language necessarily limits the address and data networks to be separate entities. The Examiner asserts they are not. Appellant disagrees with the Examiner's interpretation of how the word respectively may be construed. The Examiner alleges that the word respectively could be construed to be referring to three elements: the active devices, the memory subsystem, and an address and a data network. Appellant disagrees. Specifically, the claim recites "each node includes a plurality of active devices, a memory subsystem, and **an address network** and **a data network respectively** configured to convey address packets and data packets **between** the plurality of **active devices** and the **memory** subsystem." Appellant submits it is clear that the address network and the data network are two separate entities, because of how they are referred to (an address network and a data network), and the word respectively is used in connection with the phrase "an address network and a data

network" without a comma separating them. Appellant submits they are separate and Liencres does not teach this feature.

The Examiner further asserts that each bus cache controller must go through element 33 to get to active devices 21 and 25. Applicant submits, element 35 of Liencres is a cache controller, and NOT an active device as used in the art. A processor and an I/O device may be construed to be an active device. Accordingly as shown in Fig. 3b of Liencres, the element 33, which is a bus for reference, resides between the bus cache controller 31 and the cache controller 35. The processor 21 is on the other side of the cache controller 35. Thus Appellant submits Liencres does not teach "convey address packets and data packets **between** the plurality of **active devices** and the **memory** subsystem" as recited in claim 1.

The above notwithstanding, Appellant further disagrees with the Examiner's response in the Examiner's Answer dated March 25, 2008 regarding the node identifier. More particularly, the Examiner asserts that because the explanations fig. 1a and 1b of Liencres allegedly disclose that when the valid bit of the status bits is not set, and the shared bit is marked, this identifies that another node now owns the data and is modifying it. Appellant maintains the arguments made in the Appeal Brief and further adds that it is irrelevant that Liencres discloses that another node now owns the data. The point is Liencres DOES NOT disclose which node. Liencres only discloses that some other processor owns the data (*See* col. 2, lines 36-38), but does not dislcose "**identifies a different node** of the plurality nodes **in which the coherency unit is in a modified global access state**." The claim language DOES NOT recite "identifies that a different node …" the claim recites "identifies a different node of the plurality of nodes." Appellant submits this is not taught or disclosed in Liencres.

Lastly the claim language is not vague. The claim language is clear and definite, and refers to "**in which the coherency unit is in a modified global access state**." Appellant fails to see how this is vague.

Appellant submits claims 17 and 33 recite language that is similar to the language recited in claim 1.

Accordingly, for at least the above stated reasons, Appellant submits that the rejection of claims 1, 17, and 33 is in error and requests reversal of the rejection. The rejection of claims 2-5 and 7-16 (dependent from claim 1), claims 18-21 and 23-32 (dependent from claim 17), claims 34-37 and 39-48 (dependent from claim 33) are similarly in error for at least the above stated reasons, and reversal of the rejection is requested. Each of claims 2-5, 7-16, 18-21, 23-32, 34-37, and 39-48 recite additional combinations of features not taught or suggested in the cited art.

CONCLUSION

The Commissioner is authorized to charge the any fees that may be due to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-13501/SJC.

Respectfully submitted,

/ Stephen J. Curran /
Stephen J. Curran
Reg. No. 50,664
AGENT FOR APPELLANT

Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C.
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 853-8800

Date: May 27, 2008